CLAIMS

1. A device for addressing a shared resource, comprising:

at least one register in communication with the shared resource, the at least one register configured to hold an address to be provided to the shared resource upon receipt of a clock signal; and

a multiplexer for providing a next address to the at least one register, the multiplexer being disposed outside of a critical timing path for addressing the shared resource.

2. A device for addressing a shared resource as recited in claim 1, wherein the multiplexer is configured to receive a recirculate input, an increment input, a new address input, and a control signal, the control signal being used to determine which of the recirculate input, the increment input, and the new address input is to be provided as the next address to the at least one register.

3. A device for addressing a shared resource as recited in claim 2, wherein the new address input is provided in a time multiplexed manner to cause the at least one register to provide the address to the shared resource upon receipt of a specific clock signal.

4. A device for addressing a shared resource as recited in claim 2, wherein the new address input is provided by one of a multiple input multiplexer, a memory manager module, and a buffer allocator module, each of the multiple input multiplexer,

the memory manager module, and the buffer allocator module existing outside of the critical timing path for addressing the shared resource.

5. A device for addressing a shared resource as recited in claim 1, wherein the at least one register includes a register chain, the register chain being defined by a number of registers connected in a serial manner, the number of registers including a first register and a last register, the first register being provided with the next address from the multiplexer.

6. A device for addressing a shared resource as recited in claim 5, wherein each of the number of registers has an input and an output, the output of each register that is not the last register in the register chain being connected to the input of a sequential register in the register chain to define the serial manner of connection, the output of the last register in the register chain being connected to an input of the multiplexer.

7. A device for addressing a shared resource as recited in claim 5, wherein each of a number of portions of the shared resource is provided with one of a number of addresses from the output of the number of registers in the register chain upon receipt of the clock signal.

8. A shared memory, comprising:

a data port for sending and receiving data;

an address port for receiving an address to be used to locate data within the shared memory;

at least one register in communication with the address port, the at least one register configured to provide the address to the address port upon receipt of a clock signal; and

a multiplexer for providing a next address to the at least one register, the multiplexer being disposed outside of a critical timing path for addressing the shared memory.

9. A shared memory as recited in claim 8, wherein the multiplexer is configured to receive a recirculate input, an increment input, a new address input, and a control signal, the control signal being used to determine which of the recirculate input, the increment input, and the new address input is to be provided as the next address to the at least one register.

10. A shared memory as recited in claim 9, wherein the new address input is provided in a time multiplexed manner to cause the at least one register to provide the address to the address port upon receipt of a specific clock signal.

11. A shared memory as recited in claim 9, wherein the new address input is provided by one of a multiple input multiplexer, a memory manager module, and a buffer allocator module, each of the multiple input multiplexer, the memory manager module, and the buffer allocator module existing outside of the critical timing path for addressing the shared memory.

12. A shared memory as recited in claim 8, wherein the at least one register includes a register chain, the register chain being defined by a number of registers

connected in a serial manner, the number of registers including a first register and a last register, the first register being provided with the next address from the multiplexer.

13. A shared memory as recited in claim 12, wherein each of the number of registers has an input and an output, the output of each register that is not the last register in the register chain being connected to the input of a sequential register in the register chain to define the serial manner of connection, the output of the last register in the register chain being connected to an input of the multiplexer.

14. A shared memory as recited in claim 12, wherein each of a number of portions of the shared memory is provided with one of a number of addresses from the output of the number of registers in the register chain upon receipt of the clock signal.

15. A method for addressing a shared resource, comprising:

loading at least one register with an address to be provided to the shared resource; and

providing the address to the shared resource from the at least one register upon receipt of a clock signal.

16. A method for addressing a shared resource as recited in claim 15, further comprising:

operating a multiplexer to load the at least one register with one of a recirculated address, an incremented address, and a new address.

17. A method for addressing a shared resource as recited in claim 16, further comprising:

operating one of a multiple input multiplexer, a memory manager module, and a buffer allocator module to provide the new address to the multiplexer, wherein the multiple input multiplexer, the memory manager module, and the buffer allocator module are operated outside of a critical timing path for providing the address to the shared resource.

18. A method for addressing a shared resource as recited in claim 15, wherein a critical timing path for providing the address to the shared resource is defined by propagation of the clock signal to the at least one register and propagation of the address to the shared resource.

19. A method for addressing a shared resource as recited in claim 15, further comprising:

providing a register chain defined by the at least one register and a number of additional registers;

loading the number of additional registers with a number of additional addresses to be provided to the shared resource; and

providing each of the number of additional addresses to different portions of the shared resource from the number of additional registers upon receipt of the clock signal used to provide the address to the shared resource from the at least one register.

20. A method for addressing a shared resource as recited in claim 19, further comprising:

shifting the address and the number of additional addresses through the register chain to allow each of the address and the number of additional addresses to be provided to appropriate portions of the shared resource at a specific clock cycle.

21. A method for addressing a shared resource as recited in claim 15, wherein the shared resource is a shared memory.

22. A method for addressing a shared resource as recited in claim 15, wherein the address is provided directly to the shared resource from the at least one register upon receipt of the clock signal.